

IN THE CLAIMS:

Claim 1. (Currently Amended) A MOSFET logic circuit for performing a logic OR operation between a first input signal and inverse of a second input signal, wherein said logic circuit uses silicon-on-insulator (SOI), the circuit comprising:

a first and second transistors forming a transmission gate for outputting an intermediate signal; and

a third transistor for providing an output to be combined with said intermediate signal to create an output signal,

said first transistor receiving a the first input signal, said third transistor receiving a the second input signal, and said second transistor receiving an inverse of said second input signal,

said output signal being indicative of an OR operation performed on said first and said inverse of said second input signals, said output signal is outputted from the MOSFET logic circuit to any static CMOS logic gate.

Claim 2. (Currently Amended) The MOSFET logic circuit as in claim 1, wherein said ~~first~~ second and third transistors are PMOS transistors and said ~~second~~ first transistor is a NMOS transistor.

Claim 3. (Cancelled)

Claim 4. (Previously Presented) The MOSFET logic circuit as in claim 1, wherein the first input signal is provided to a source of said first and second transistors, the inverse of the second input signal is provided to a gate of the second transistor, and the second input signal is provided to a gate of the first transistor.

Claim 5. (Previously Presented) The MOSFET logic circuit as in claim 1, wherein the second input is provided to a gate of the third transistor.

Claim 6. (Cancelled)

Claim 7. (Previously Presented) The MOSFET logic circuit as in claim 1, wherein when the inverse of the second input signal has a logic LOW level, the output of the MOSFET logic circuit is an output signal of the transmission gate.

Claim 8. (Previously Presented) The MOSFET logic circuit as in claim 1, wherein the third transistor is a pull-up transistor, and when the inverse of the second input signal has a logic HIGH level, the output of the MOSFET logic circuit has a voltage level approximately equal to a drain of the third transistor, which pulls up the output signal from the transmission gate to a logic HIGH level.

Claim 9. (Previously Presented) The MOSFET logic circuit as in claim 1, wherein a delay of the MOSFET logic circuit is one of a delay of the transmission gate formed by first and second transistors, and a delay of the third transistor.

Claim 10. (Currently Amended) A logic OR circuit comprising:
a transmission gate for outputting a first intermediate output signal, said transmission gate being formed by a pMOS transistor receiving a first input signal and a nMOS transistor receiving a said first input signal, wherein a gate of said pMOS transistor receives an inverse of a second input signal; and

a pull-up pMOS transistor receiving said second input signal, said pull-up pMOS transistor providing a second intermediate output signal for combining with said first intermediate output signal to create an OR output signal,

wherein said OR output signal is indicative of an OR operation performed on said first and the ~~reverse~~ inverse of the second input signals, said OR output signal is outputted from the OR logic circuit to any static CMOS logic gate.